Abstracts

Development of SOI based MMICs for wireless LAN applications

S. Pinel, S. Chakraborty, S. Venkataraman, R. Bhatia, S. Mandal, S. Nuttinck, B. Larson and J. Laskar. "Development of SOI based MMICs for wireless LAN applications." 2002 MTT-S International Microwave Symposium Digest 02.2 (2002 Vol. II [MWSYM]): 1053-1056 vol.2.

Due to its improved RF performances over conventional CMOS, SOI technology is a promising candidate for front-end wireless transceiver circuits. This paper demonstrates the development of fully on-chip integrated SOI based MMICs for IEEE 802.11a standard. A modified BSIM model is developed to predict small signal RF behavior. The development of high Q on-chip inductor design and modeling is detailed. The low noise amplifier, implemented in a commercially available 0.35 /spl mu/m SOI MOSFET process, is both input and output 50 Ohms matched and operates in C-band. It exhibits a forward gain (S21) of 10.5 dB with a noise figure of 4.5 dB while drawing 15 mA from a 1.8 V supply. The doubly balanced Gilbert cell topology mixer exhibits a peak gain of 7.5 dB and IIP3 of +11 dBm. It consumes about 11 mA from a 3.3 V supply. To the best of our knowledge this research is the first report of SOI based implementation of MMICs for C-band wireless applications.

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